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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/879,658	06/11/2001	Takahide Ohkami	264/087	2956

34313 7590 04/22/2005

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/879,658	OHKAMI, TAKAHIDE	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 February 2005.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 and 10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 10 is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11 June 2001 and 22 February 2005 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/3/05.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-7 and 10 of U.S. Application 09/879,658, originally filed on 06/11/2001 are presented for examination. The application claims priority to provisional application 60/242,407, filed on 10/20/2000. Claims 8-9 have been cancelled in Applicant's amendment filed 02/22/2005. Claims 1-6 and 10 have been amended.
2. Applicant's amendment necessitated the new grounds of rejection presented in this Office Action. Accordingly, this Office Action is made final.

Drawings

3. The new drawing of Fig.19 was received on 2/22/2005. Applicants argue in p.8 of the amendment filed on 2/22/2005 that support for this Fig.19 exists in paragraphs 46, 48, 49, and 50 of the specification. Examiner finds Applicant's argument to be persuasive, and is entering Figure 19 into the record.

Claim Objections

4. Claim 1 is objected to because of the following informalities: line 9 in the amended claim contains the following typographical error: "... in the user's logic **desgin** ...". Appropriate correction is required.

5. The title is objected to because it contains the following typographical error: "Hardware-Assisted **Disign** ...". Appropriate correction is required.

Allowable Subject Matter

6. Claim 10 is allowed. In the previous Office Action, Claim 10 was objected to as being dependent upon a rejected base claim. The cited prior art (Sample, Koch, Patel, X.25) does not expressly teach, either individually or in combination, the following limitations:

> creating a finite state machine to indicate that the packet-based protocol logic is in either non-memory mode, continuous memory write mode, or continuous memory read mode; and
>
> creating a state transition control that selects said non-memory mode when said continuous memory operation ends, said state transition control further selecting said continuous memory write mode when said continuous memory write operation is initiated, said state transition control further selecting said continuous memory read mode when said continuous memory read operation is initiated.

Applicants have amended Claim 10 to incorporate the limitations of base Claim 9.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. The prior art used for these rejections is as follows:

9. Sample et al., U.S. Patent 5,841,967. (Henceforth referred to as "**Sample**").

10. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

11. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Sample.

12. In regards to Claim 1, Sample teaches the following limitations:

> 1. (Currently Amended) A method for compiling a user's logic design for implementation into a functional verification system such that communication bandwidth is increased between the functional verification system and a host workstation by allowing for greater read and write access to memories and registers in the user's logic design, comprising;
>
> identifying all of the memories and registers in the user's logic design;

Sample teaches (col.3, lines 45-50): "Accordingly, a general object of the present invention is to provide an apparatus and method for efficiently coupling simulation and emulation of a logic design, so that the overhead of event transfer between the simulated and the emulated design portions is minimized."

Furthermore, Sample teaches (col.4, lines 59-60): "Fig.1 shows the preferred embodiment of the logic verification system."

Sample also teaches (col.5, lines 23-30): "FPGA devices 10 emulate the logic circuit portions under verification represented as the interconnection of components, as disclosed in Butts et al., U.S. Patent No. 5,036,473. Simulation modules 14 simulate the logic circuit portions under verification which may be represented by behavioral descriptions."

Examiner finds that memories and registers in a user's logic design inherently can be represented by behavioral descriptions, and therefore would be simulated by Sample's simulation modules 14.

> synthesizing accessibility logic into the user's logic design such that the user's logic design supplemented by said accessibility logic,

Sample teaches (col.4, lines 60-65): "The system includes one or more reconfigurable logic components which may be programmable gate array ("FPGA") devices 10 interconnected using the programmable interconnect 12. The interconnect 12 can be programmed to create an arbitrary connection between any number of inputs or outputs of the devices connected to it."

Examiner finds that Sample's "programmable interconnect" corresponds to Applicant's "accessibility logic."

> said accessibility logic creating access ports to the memories and registers <u>in the user's logic design,</u>

Sample teaches (col.5, lines 29-40): "The hardware logic implemented in FPGA 22 selects the behavioral fragments to be executed and the order of execution ... FPGA devices 22 also communicate the signal values shared between the behavioral description portion and those design portions represented by the interconnection of components."

> <u>the access ports facilitating writing of data received from the host workstation to the memories and registers in the user's logic design,</u>
>
> <u>said access ports further facilitating reading of data stored in the memories and registers in the user's logic design for transfer to the host workstation</u>.

Sample teaches (col.5, lines 55-65): "The system controller 26 performs the functions of downloading configuration data into the FPGA devices 10, 22, downloading the executable data into the random access memory devices 20, starting the logic verification system, communicating data between the logic verification system and the host workstation (not shown). The system controller 26 is implemented using a commercial embedded controller board or by any other means known to those skilled in the art."

13. In regards to Claim 2, Sample teaches the following limitations:

> 2. (Currently Amended) The method of claim 1 further comprising the step of assigning a unique identifier to each of the memories and registers in the user's <u>logic</u> design.

Sample teaches (col.6, lines 22-30): "Rather than routing the signals shared between the multiple simulation modules 14 through programmable interconnect 12, such signals can be communicated in a serial fashion, one signal at a time, over the global-event-communication bus. The simulation module 14, that serves as a transmitter of a new signal value, sets some of the signal lines 30 to represent the serial number of such signal and its new value. This information reaches all other simulation modules 14 and is captured as necessary."

Examiner interprets that the "serial number of such signal" corresponds to a memory address, because information transmitted over buses inherently includes address and value. Therefore, Examiner finds that Sample's "serial number of such signal" corresponds to the Applicant's claimed "unique identifier" for each memory and register.

14. In regards to Claim 3, Sample teaches the following limitations:

> 3. (Currently Amended) The method of claim 2 wherein said accessibility logic comprises selecting logic,

> said selecting logic adapted to receive said unique identifier and select a particular one of the memories and registers in the user's logic design.

Sample teaches (col.6, lines 22-30): "Rather than routing the signals shared between the multiple simulation modules 14 through programmable interconnect 12, such signals can be communicated in a serial fashion, one signal at a time, over the global-event-communication bus. The simulation module 14, that serves as a transmitter of a new signal value, sets some of the signal lines 30 to represent the serial number of such signal and its new value. This information reaches all other simulation modules 14 and is captured as necessary."

Examiner interprets that the "serial number of such signal" corresponds to a memory address, because information transmitted over buses inherently includes address and value. Therefore, Examiner finds that Sample's "serial number of such signal" corresponds to the Applicant's claimed "unique identifier" for each memory and register.

Moreover, Examiner finds that Sample's teaching that "This information reaches all other simulation modules 14 and is captured as necessary" corresponds to the claimed "said selecting logic adapted to receive said unique identifier and select a particular one of the memories and registers in the user's logic design."

15. In regards to Claim 4, Sample teaches the following limitations:

> 4. (Currently Amended) The method of claim 3 wherein said accessibility logic comprises logic to read from or write to said particular one of the memories and registers in the user's logic design.

Sample teaches (col.6, lines 51-56): "While executing the behavioral description fragments, the microprocessors 16 need to set the new values to the variables that describe the current state of the logic design being simulated. Those variables that are locally used in only one simulation module 14 are represented by appropriate locations in the random access memory device 20."

16. In regards to Claim 5, Sample teaches the following limitations:

> 5. (Currently Amended) The method of claim 4 wherein said accessibility logic comprises decode logic that receives commands from a host and controls execution of reading and writing data to the memories and registers in the user's logic design.

Sample teaches (col.7, lines 6-8): "In response, the operation decoder 42 enables the variable selector 44 which then recognizes the combination of values on lines 38 as indicative of a particular variable."

17. In regards to Claim 6, Sample teaches the following limitations:

6. (Currently Amended) A hardware-assisted design verification system for verifying a target <u>logic circuit</u> design, said verification system having a host workstation in communication with a hardware accelerator, the target <u>logic circuit</u> design comprising <u>Boolean logic gates,</u> registers and memories, the host workstation loading data to or unloading data from the registers and memories, comprising:

protocol logic synthesized into the <u>target</u> logic circuit <u>design</u>, said protocol logic comprising:

See Sample, col.5, lines 40-65. Note also that Sample teaches a token ring protocol in col.6, lines 32-42.

an incoming packet register in communication with said host workstation<u>, said incoming packet register storing packets that include data and commands communicated from the host workstation</u>;

an outgoing packet register in communication with said host workstation, <u>said outgoing packet register storing packets that include data to be communicated to the host workstation;</u>

Sample teaches (col.5, lines 55-65): "The system controller 26 performs the functions of downloading configuration data into the FPGA devices 10, 22, downloading the executable data into the random access memory devices 20, starting the logic verification system, communicating data between the logic verification system and the host workstation (not shown). The system controller 26 is implemented using a commercial embedded controller board or by any other means known to those skilled in the art."

Examiner finds that Sample's "random access memory devices" correspond to the claimed "packet registers".

command decode logic, said command decode logic decoding <u>said</u> command<u>s</u> in said incoming packet register to identify a particular operation, register or memory location in said target <u>logic circuit</u> design, <u>where said particular operation can comprise a write command and where said particular operation can also comprise a read command;</u>

Sample teaches (col.7, lines 6-8): "In response, the operation decoder 42 enables the variable selector 44 which then recognizes the combination of values on lines 38 as indicative of a particular variable."

write command execution logic to write data stored in said incoming packet register into said register or memory location in said target <u>logic circuit</u> design for a write command decoded at said command decode logic;

See Sample, col.7, lines 24-32.

> read command execution logic to read data from said register or memory location in said target logic circuit design and store said data in said outgoing packet register for a read command decoded at said command decode logic; and

See Sample, col.7, lines 33-40.

> interface logic interfacing said registers and memories in said target logic circuit design.

Sample teaches (col.4, lines 60-65): "The system includes one or more reconfigurable logic components which may be programmable gate array ("FPGA") devices 10 interconnected using the programmable interconnect 12. The interconnect 12 can be programmed to create an arbitrary connection between any number of inputs or outputs of the devices connected to it."

Examiner finds that Sample's "programmable interconnect" corresponds to Applicant's "accessibility logic."

18. In regards to Claim 7, Sample teaches the following limitations:

> 7. (Original) The hardware-assisted design verification system of claim 6, wherein said protocol logic includes logic to determine whether data from said incoming packet register is new and control activation of command decoding and execution.

Sample teaches (col.7, lines 6-8): "In response, the operation decoder 42 enables the variable selector 44 which then recognizes the combination of values on lines 38 as indicative of a particular variable."

Conclusion

19. Applicant's arguments filed 2/22/2005 have been fully considered but they are not persuasive.

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is

filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached at (571) 272-3716.

Any response to this office action should be faxed to (703) 872-9306, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
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Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

April 15, 2005

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER